NIT-201-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Prior Application:	N. KATOH et al Serial No. 10/084,435 Filed: February 28, 2002
Group Art Unit:	2825
Examiner:	P. Kik
For:	SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, STORAGE MEDIUM ON WHICH CELL LIBRARY IS STORED AND DESIGNING METHOD FOR SEMICONDUCTOR INTEGRATED CIRCUIT

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Mail Stop Patent Application
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure, the Applicants inform the Examiner of the documents cited during prosecution of the parent application, U.S. Serial No. 10/084,435.

The Applicants request the Examiner to initial and return a copy of the attached PTO-1449 form as an indication that the references have been considered.

Respectfully submitted,

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Attorney of Record

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Date: April 20, 2004

FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. NIT-201-03	SERIAL NO.
LIST OF DOCUMENTS CITED BY APPLICANT *(Use several sheets if necessary)*		APPLICANT N. KATOH et al	
		FILING DATE April 20, 2004	GROUP

U.S. PATENT DOCUMENTS

* EXAMINER INITIAL		DOCUMENT	DATE	NAME	CLASS	SUBCLASS	FILING DATE *(If Appropriate)*
	AA	5,774,367	06/30/98	Reyes et al			
	AB	5,614,847	03/1997	Kawahara et al			
	AC	6,118,309	09/2000	Akamatsu et al			
	AD	6,222,410	04/2001	Seno			
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		DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	AL	8-274620	10/18/96	Japan			☐	☐
	AM	9-45785	02/14/97	Japan			☐	☐
	AN	9-205148	08/1997	Japan			☐	☐
	AO	9-319775	12/1997	Japan			☐	☐
	AP						☐	☐

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	AR		S. Mutoh et al, "1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS", IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. 30,
			No. 8, August 1995, pp. 847-854.
	AS		T. Sakata et al, "Subthreshold-Current Reduction Circuits for Multi-Gigabit DRAM's", 1993 SYMPOSIUM ON VLSI CIRCUITS DIGEST OF TECHNICAL PAPERS,
			May 1993, pp. 45-46.
	AT		Uebel et al, "A Timing Model for VLSI CMOS Circuits Verification and Optimization", 1994 IEEE International Symposium on Circuits and Systems,
			Vol. 1, May 30, 1994, pp. 439-442.

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	AR		Daga et al, "Delay Modelling Improvement for Low Voltage Applications", Proceedings of European Design Automation Conference, Sept. 18, 1995,
			pp. 216-221.
	AS		Rofail et al, "Delay Time Sensitivity Analysis of Multi-Generation BiCMOS Digital Circuits", IEEE Proceedings of Circuits, Devices and Systems,
			Vol. 144, No. 2, Apr. 1997, pp. 60-67.
	AT		NA84035023, "Logic Signal Delay Circuit", IBM Technical Disclosure Bulletin,
			Vol. 26, No. 10A, Mar. 1984, pp. 5023-5025.

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	AM						☐	☐
	AN						☐	☐
	AO						☐	☐
	AP						☐	☐

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	AR		NB9001420, "Buffer Circuit with Delayed Rising or Falling Transition for Pulsewidth Skew Control", IBM Technical Disclosure Bulletin, Vol. 32, No. 8B, Jan. 1990, pp. 420-421.
	AS		NN87044929, "High Noise Immunity CMOS Driver", IBM Technical Disclosure Bulletin, Vol. 29, No. 11, Apr. 1987, pp. 4929-4930.
	AT		

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